AMENDMENTS TO THE CLAIMS

1. (original) A peripheral device having bus isolation and comprising:

a signal translator receiving a plurality of input/output (I/O) signals from a peripheral device logic and for translating between said plurality of I/O signals and a plurality of bus signals which are fewer in number than said plurality of I/O signals;

a first unidirectional to bi-directional converter coupled to said signal translator;

an optical isolation barrier coupled to said first unidirectional to bi-directional converter via first unidirectional signal lines;

a second unidirectional to bi-directional converter coupled to said optical isolation barrier via second unidirectional signal lines that are electronically isolated from said first unidirectional lines, said second converter for generating a plurality of isolated bus signals; and

an interface for interfacing with a serial bus using said plurality of isolated bus signals.

2. (original) The peripheral device of Claim 1 wherein said translator circuit is a microcontroller which signals bus communication direction by a dedicated bus direction signal pin that is coupled to both of said first and second unidirectional to bi-directional converters.

3. (original) The peripheral device of Claim 2 wherein said microcontroller controls the direction of transmission of said first and said second unidirectional to bi-directional converters via said bus direction signal.

4. (original) The peripheral device of Claim 1 wherein said optical isolation barrier electronically isolates said peripheral device logic from said serial bus.

5. (original) The peripheral device of Claim 1 wherein said first unidirectional to bi-directional converter and said second unidirectional to bi-directional converter comprise separate ground potentials.

6. (original) The peripheral device of Claim 1 wherein said plurality of bus signals comprises differential data lines.

7. (original) The peripheral device of Claim 1 wherein said serial bus is substantially compliant with the USB (Universal Serial Bus) standard.

8. (original) The peripheral device of Claim 2 where said signal pin comprises a logic high driver and an external pull down resistor.

9. (currently amended) A peripheral device having bus isolation and comprising:

a microcontroller receiving a set of input/output (I/O) signals from peripheral device logic and for translating between said set of I/O signals and a

set of bus signals, wherein said set of bus signals are fewer in number than said set of I/O signals;

a first unidirectional to bi-directional converter coupled to said microcontroller;

an optical isolation barrier comprising a plurality of optical isolating devices for electrically isolating said bus signals from ~~said~~ a serial bus, said optical isolating barrier coupled to said first unidirectional to bi-directional converter via first unidirectional signal lines;

a second unidirectional to bi-directional converter coupled to said optical isolation barrier via second unidirectional signal lines and for generating a set of isolated bus signals; and

a serial bus interface for interfacing with said serial bus using said set of isolated bus signals.

10. (original) The peripheral device of Claim 9 wherein said microcontroller signals communication direction by a dedicated bus direction signal pin.

11. (original) The peripheral device of Claim 10 wherein said microcontroller controls the direction of transmission of said first and said second unidirectional to bi-directional converters via said bus direction signal pin which is coupled to said first and second unidirectional to bi-directional converters.

12. (original) The peripheral device of Claim 9 wherein said optical isolation barrier electrically isolates said peripheral device logic from said serial bus.

13. (original) The peripheral device of Claim 9 wherein said first unidirectional to bi-directional converter and said second unidirectional to bi-directional converter comprise separate ground potentials.

14. (currently amended) The peripheral device of Claim 9 wherein said ~~plurality of I/O~~ set of isolated bus signals comprises of differential data lines.

15. (original) The peripheral device of Claim 9 wherein said serial bus is substantially compliant with the USB (Universal Serial Bus) standard.

16. (currently amended) A method for isolating a peripheral device from a host device comprising the steps of:

a) translating between input output (I/O) signals of peripheral device logic of said peripheral device and serial bus signals wherein said serial bus signals are fewer in number than said I/O signals;

b) electronically isolating said bus signals to generate isolated bus signals comprising:

b1) translating between said serial bus signals and first unidirectional signals;

b2) electrically isolating said first unidirectional signals and second unidirectional signals using optical isolation elements; and

b3) translating between said second unidirectional signals and said isolated bus signals; wherein said step a) is performed by a microcontroller and wherein said step b1) is performed by a first unidirectional to bi-directional converter based on a bus direction signal generated by said microcontroller and wherein said step b3) is performed by a second unidirectional to bi-directional converter based on said bus direction signal; and

c) interfacing said isolated bus signals over said serial bus to electrically isolate said peripheral device logic from said serial bus.

17. (cancelled)

18. (currently amended)A method as described in Claim ~~17~~ 16 wherein said bus signals and said isolated bus signals comprise bi-directional signals.

19. (original) A method as described in Claim 18 wherein said bus signals further comprise differential data signals.

20. (original) A method as described in Claim 16 wherein said step a) is performed by a microcontroller.

21. (cancelled)